WHAT IS CLAIMED IS:

1. A graphics system comprising:

a refresh address generator, operable alternatively in column-forward and column-reverse modes, for generating and applying to an image buffer memory refresh address signals that specify memory addresses successively associated with memory-location columns in each of a plurality of successive memory-location rows, wherein the memory addresses that the refresh address signals specify increase within a memory-location row when the refresh-address generator is operating in its column-forward mode and decrease within a memory-location row when the refresh-address generator is operating in its column-reverse mode.

2. A graphics system as defined in claim 1 wherein the refresh-address generator includes:

A) an output latch that receives an output-latch input and generates as the refresh-address output a signal representing a value determined by the value of the output-latch input at the last of a sequence of clock times; and

B) a next-address multiplexer that alternatively couples a first-column signal and a next-column signal to the output latch as its output-latch input.

3. A graphics system as defined in claim 2 wherein the refresh-address generator includes:

A) an increment circuit that generates an increment output representing an address one greater than the value that the refresh-address output represents;

B) a decrement circuit that generates a decrement output representing an address one less than the value that the refresh-address output represents; and

C) a next-column multiplexer that generates the next-column signal by forwarding the increment output when the refresh-address generator is in its column-forward mode and by forwarding the decrement output when the refresh-address generator is in its column-reverse mode.

4. A graphics system as defined in claim 3 wherein the refresh-address generator additionally operates alternatively in row-forward and row-reverse modes and the memory addresses that the refresh address signals specify increase between memory-location rows when the refresh-address generator is operating in its row-forward mode and decrease between memory-location rows when the refresh-address generator is operating in its row-reverse mode.

5. A graphics system as defined in claim 2 wherein the refresh-address generator additionally operates alternatively in row-forward and row-reverse modes and the memory addresses that the refresh address signals specify increase between memory-location rows when the refresh-address generator is operating in its row-forward mode and decrease between memory-location rows when the refresh-address generator is operating in its row-reverse mode.

6. A graphics system as defined in claim 5 wherein the refresh-address generator includes:

A) a first-column latch that receives a first-column-latch input and generates as the first-column signal a signal representing a value determined by the value of the first-column-latch input at the last of a sequence of row-clock times;

B) a sum circuit that generates a sum output representing an address greater by a row offset than the value that the first-column signal represents;

C) a difference circuit that generates a difference output representing an address less by the row offset than the value that the first-column signal represents;

D) a next-row multiplexer that generates a next-row signal by forwarding the sum output when the refresh-address generator is in its row-forward mode and by forwarding the difference output when the refresh-address generator is in its row-reverse mode; and

E) a row-signal coupling circuit that forwards the next-row signal to the first-column latch as the first-column-latch input.

7. A graphics system as defined in claim 6 wherein the row-signal coupling circuit comprises a row-start multiplexer that alternatively couples a start-address signal and the next-row signal to the first-column latch as the first-column-latch input.

8. A graphics system as defined in claim 1 wherein the refresh-address generator additionally operates alternatively in row-forward and row-reverse modes and the memory addresses that the refresh address signals specify increase between memory-location rows when the refresh-address generator is operating in its row-forward mode and decrease between memory-location rows when the refresh-address generator is operating in its row-reverse mode.

9. A graphics system comprising:

refresh logic, operable alternatively in row-forward and row-reverse modes, for generating and applying to an image buffer memory refresh address signals that specify memory addresses successively associated with memory-location columns in each of a plurality of successive memory-location rows, wherein the memory addresses that the refresh address signals specify increase between memory-location rows when the refresh-address generator is operating in its row-forward mode and decrease between memory-location rows when the refresh-address generator is operating in its row-reverse mode.

10. A graphics system as defined in claim 9 wherein the refresh-address generator includes:

A) an output latch that receives an output-latch input and generates as the refresh-address output a signal representing a value determined by the value of the output-latch input at the last of a sequence of clock times; and

B) a next-address multiplexer that alternatively couples a first-column signal and a next-column signal to the output latch as its output-latch input.

11. A graphics system as defined in claim 10 wherein the refresh-address generator includes:

A) a first-column latch that receives a first-column-latch input and generates as the first-column signal a signal representing a value determined by the value of the first-column-latch input at the last of a sequence of row-clock times;

B) a sum circuit that generates a sum output representing an address greater by a row offset than the value that the first-column signal represents;

C) a difference circuit that generates a difference output representing an address less by the row offset than the value that the first-column signal represents;

D) a next-row multiplexer that generates a next-row signal by forwarding the sum output when the refresh-address generator is in its row-forward mode and by forwarding the difference output when the refresh-address generator is in its row-reverse mode; and

E) a row-signal coupling circuit that forwards the next-row signal to the first-column latch as the first-column-latch input.

12. A graphics system as defined in claim 11 wherein the row-signal coupling circuit comprises a row-start multiplexer that alternatively couples a start-address signal and the next-row signal to the first-column latch as the first-column-latch input.

13. A graphics system as defined in claim 9 wherein the refresh logic additionally operates alternatively in column-forward and column-reverse modes, for generating and applying to an image buffer memory refresh address signals that specify memory addresses successively associated with memory-location columns in each of a plurality of successive memory-location rows, wherein the memory addresses that the refresh address signals specify increase within a memory-location row when the refresh-address generator is operating in its column-forward mode and decrease within a memory-location row when the refresh-address generator is operating in its column-reverse mode.